Appln. No. 10/628,782
Petition to Make Special Under
MPEP § 708.2, VIII

PATENT
Attorney Docket No. 81940.0052
Customer No. 26021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Seiji KANEKO, et al.
Serial No.: 10/628,782
Filed: July 28, 2003
For: DISK ARRAY DEVICE, METHOD FOR CONTROLLING THE DISK ARRAY DEVICE AND STORAGE SYSTEM

Art Unit: 2655
Examiner: Not Yet Assigned
Confirmation No.: 5210

I hereby certify that this correspondence is being transmitted via facsimile to (703) 872-9306:
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450 on

September 17, 2004
Date of Deposit
Rhonda Hurt
Name
Rhonda Hurt 09/17/04
Signature Date

PETITION TO MAKE SPECIAL UNDER MPEP § 708.2, VIII

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

I. Petition

Applicant hereby petitions to make this new application, which has not received any examination by the Examiner, special.

II. Claims

Check and complete all applicable items (a) through (c).

(a) x All the claims in this case are directed to a single invention.

(b) x If the Office determines that all the claims presented are not obviously directed to a single invention, applicant will make an election, without traverse, as a prerequisite to the grant of special status.

(c) x The applicant submits a preliminary amendment concurrently.

III. Search

A. Check all applicable items (d) through (g)

A search has been made by

(d) __ the inventor

(e) __ attorney

(f) x professional searcher (search report is attached)

(g) __ foreign Patent Office

in the following:

B. Complete all applicable items below

(h) x field of search: The field of search is described in the attached Search Report by the professional searcher.

Class(es):	Subclass(es):
711;	112, 113, 114, and 167
714;	5

(i) __ publications:

(j) __ foreign patents:

(k) __ search by corresponding foreign Patent Office or at the former International Patent Institute at The Hague, Netherlands

C. Copy of references

There is submitted herewith an Information Disclosure Statement and Form PTO-1449 listing the references identified by the search. Copies of the references are not submitted herewith as the requirement is waived under 37 CFR 1.98.

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D. Detailed discussion of the most pertinent references

There is submitted herewith a detailed discussion of the references deemed to be most pertinent, which discussion particularly points out how the claimed subject matter is distinguishable over the references.

E. Fee

The fee required by 37 CFR 1.17(i)(2) is to be paid by

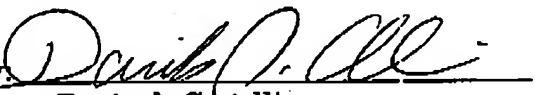
_ the attached check for $ 130.00.

x If there are any additional fees due in connection with the filing of this petition, please charge the fees to our Deposit Account No. 50-1314. A duplicate copy of this Petition is enclosed.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Dated: September 16, 2004

By: 
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DETAILED DISCUSSION OF THE MOST PERTINENT REFERENCES AND COMPARISON TO THE PRESENT INVENTION

IV. Field of the Invention:

The present invention relates to a disk array device, a control method for the disk array device, and a storage system.

V. Related Background Art:

A common disk array device has a structure in which a disk adapter that controls input/output of data to disk drives, an input/output channel that controls connection with a host computer, and a cache memory are connected to one another via a network switch provided inside the disk array device.

As a result, the input/output channel, the disk adapter and the cache memory compete for traffic within the network switch of the disk array device, which increases the usage rate of the network switch, which in turn reduces the response speed to the host computer.

VI. The References:

Below is a discussion of the references deemed to be most pertinent.

A. The Shimada Reference:

U.S. Patent App. Pub. No. 2003/0221062 (Shimada) discloses enlarging a disk array system by increasing the number of input/output channels and the number of disk adapters. (*See, Shimada, Page 1, paragraph [0010]*). According to Shimada, the disk array system has a plurality of input/output channels used for communications with host computers, cache memories coupled to each of the plurality of input/output channels and used to store input/output data temporarily, one or more disk drives, one or more disk adapters coupled to the one or more disk drives, and one or more networks used to couple the plurality of input/output channels to the one or more disk adapters. (*See, Shimada, Figure 1; Pages 2-3, paragraphs [0032]-[0059]).*

B. The Aruga Reference:

U.S. Patent App. Pub. No. 2004/0024951 (Aruga) discloses a switch connection having a protocol converter for converting a protocol used between a disk drive unit and a controlling device to allow the disk drive unit and the controlling device to be connected one to one in a switching connection. (*See, Aruga, Page 1, paragraph [0014]).* According to Aruga, if data in the cache memory is to be transferred to a host computer, then the data in the cache will be transferred to the host by the host interface controller. If the data to be transferred to the host is not in the cache memory, then the disk drive interface controllers will read split data segments out of the disk drive group, concatenate the split data segment blocks in the parity data generator, and store the complete data temporarily in the cache memory; the host interface controller will transfer the data to the host. (*See, Aruga; Figure 1; Page 2, paragraph [0028]).*

C. The Hirano Reference:

U.S. Patent App. Pub. No. 2003/0120862 (Hirano) discloses a controlling method for a storage apparatus and disk device. (*See, Hirano, Page 1, paragraphs [0008]-[0009]).* According to Hirano, when an upper controller receives data from an external device, the upper controller interrupts an MPU and sends a report upon receipt. The MPU decodes the signal and determines the type of access and sends an instruction to the upper controller to transfer the data and region-specifying information corresponding to two regions of a cache memory. (*See, Hirano; Figure 2; Page 2, paragraph [0024]).*

D. The Mason Reference:

U.S. Patent No. 5,884,098 (Mason) discloses a disk controller having a host I/O port connected through a host I/O processor to a front end cache. (*See, Mason, Col. 5, lines 11-14).* The front end cache is connected through a disk array I/O processor to an

array of disks via a physical disk handler, a back end cache, and a disk I/O port. (*See, Mason, Col. 5, lines 14-23).* According to Mason, there is only one physical cache memory used for both the front end cache and the back end cache. (*See, Mason, Col. 5, lines 55-56).* The front end cache and the back end cache are separate software processes or subroutines. (*See, Mason, Col. 5, lines 24-30).*

VII. The Present Invention is Patentably Distinguishable Over the Above References

A. One Embodiment of the Present Invention:

The present invention seeks to address the above deficiencies of the prior art. According to an embodiment of the present invention, independent Claim 1 defines a disk array device that includes a plurality of input/output channels that receive data input/output requests from at least one external device. The disk array device includes a plurality of cache memories provided for the corresponding respective input/output channels. Each of the cache memories are connected to each of the corresponding respective input/output channels. The disk array device includes a disk drive device. The disk array device includes a disk control module that performs data input/output to and from the disk drive device. The disk array device includes at least one communication module that communicatively connects the input/output channels with the disk control module. The disk array device includes a control module that controls, upon receiving a data input/output request from the at least one external device, an execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing to maintain consistency of data stored in each of the cache memories.

With such a device in accordance with the embodiment described above, the consistency maintaining processing of the present invention includes invalidating

similar pre-update data stored in one or more of the cache memories that is stored in the same storage region as the storage region of the disk drive where the data to be updated is stored. Additionally, the consistency maintaining processing of the present invention includes updating the data in a cache memory as well as the same pre-update data stored in another cache memory that is stored in the same storage region of the disk drive where the data to be updated is stored.

The consistency maintaining module of the present invention allows processing of data, stored in multiple caches to be updated, in a more reliable manner and improves the efficiency of the disk array device. *(See, Specification, Page 6, lines 10-22 to Page 7, lines 1-5).*

By controlling the execution order of a response processing to the host computer for an input-output request and by controlling the order of execution depending on whether consistency must be maintained or not, the disk array device can be used efficiently. In one aspect, the execution order is controlled depending on which operation mode the input/output channel that received the data input/output request from the external device is operating. *(See, Specification, Page 6, line 22 to Page 7, line 8 and Page 8, lines 7-9).*

B. Distinction over the cited references

The noted references do not disclose or suggest the above features of the present invention. In particular, the noted references do not disclose or suggest, "a control module that controls, upon receiving a data input/output request from the at least one external device, an execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing to maintain consistency of data stored in each of the cache memories," as required by amended independent Claim 1 of the present invention.

Shimada teaches a disk array system having a plurality of input/output channels used for communications with host computers, cache memories coupled to each of the plurality of input/output channels and used to store input/output data temporarily, one or more disk drives, one or more disk adapters coupled to the one or more disk drives, and one or more networks used to couple the plurality of input/output channels to the one or more disk adapters. *(See, Shimada; Figure 1; Page 1, paragraph [0011]).* According to Shimada, a processor executes a control program stored in a local memory to execute the functions of the input/output channels. *(See, Shimada; Figure 2; Page 3, paragraph [0066]).* A processor executes a control program stored in a local memory to execute the functions of the disk adapters. *(See, Shimada; Figure 3; Page 3, paragraph [0073]).* However, Shimada does not teach or suggest a control module that controls an execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing to maintain consistency of data stored in each of the cache memories as required by amended independent Claim 1.

Aruga teaches a switch connection having a protocol converter for converting a protocol used between a disk drive unit and a controlling device to allow the disk drive unit and the controlling device to be connected one to one in a switching connection. *(See, Aruga, Page 1, paragraph [0014]).* According to Aruga, a switch controller develops a protocol control or conversion by assigning identification numbers to storage regions within disk drive units so that a disk drive interface controller can establish a connection to the particular disk drive unit with a particular identification number. *(See, Aruga, Page 2, paragraph [0032]).* Aruga does not teach or suggest a control module that controls an execution order of a response processing to respond to the at least one external device according to the data input/output request and a

consistency maintaining processing to maintain consistency of data stored in each of the cache memories as required by amended independent Claim 1.

Hirano teaches a disk array device connected to an external device, such as a host computer, and includes a disk controller and a plurality of disk drives controlled by the disk controller. (*See, Hirano, Page 2, paragraph [0021]).* According to Hirano, the disk controller includes a microprocessor (MPU), a cache memory, a data controller for controlling the cache memory, an upper controller that coordinates input/output control of data between the external device and the data controller, and a drive controller controlling each disk drive. (*See, Hirano, Page 2, paragraph [0021]).* In addition, according to Hirano, the disk controller writes data in duplicate to a plurality of regions in the cache memory and then also writes the same data to storage devices. (*See, Hirano, Page 2, paragraphs [0026]-[0028]).* Hirano does not, however, teach or suggest a control module that controls an execution order of a response processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing to maintain consistency of data stored in each of the cache memories as required by amended independent Claim 1.

Mason teaches a disk controller having a host I/O port connected through a host I/O processor to a front end cache. (*See, Mason, Col. 5, lines 11-14).* The front end cache is connected through a disk array I/O processor to an array of disks via a physical disk handler, a back end cache, and a disk I/O port. (*See, Mason, Col. 5, lines 14-23).* According to Mason, a preferred communication path between the host I/O processor and the disk array processor is a common data structure residing in a common control store accessible to both the front end cache and the back end cache; the structure is created when an I/O request is received and destroyed when the I/O request is complete. (*See, Mason, Figure 2; Col. 7, lines 13-17).* Mason does not teach or even suggest a control module that controls an execution order of a response

processing to respond to the at least one external device according to the data input/output request and a consistency maintaining processing to maintain consistency of data stored in each of the cache memories as required by amended independent Claim 1.

Since the noted references fail to disclose, teach, or suggest the above features as recited in amended independent Claim 1, these references cannot be said to anticipate nor render obvious the invention which is the subject matter of that claim.

Accordingly, amended independent Claim 1 is believed to be in condition for allowance and such allowance is respectfully requested. The Applicants also respectfully submit that independent Claims 10, 18, and 24 are believed to be allowable for at least the same reasons as those discussed in connection with amended independent Claim 1.

The remaining claims 2-4, 6-9, 11-17, and 19-23 depend either directly or indirectly from amended independent Claim 1 or independent Claims 10, 18, and 24 and recite additional features of the invention which are neither disclosed nor fairly suggested by the noted references and are, therefore, also believed to be in condition for allowance.

VIII. Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance and such action is respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6809 to discuss the steps necessary for placing the application in condition for allowance.

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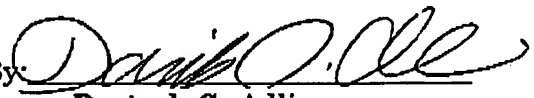
If there are any fees due in connection with the filing of this petition, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: September 17, 2004

By: 

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